AMENDMENT TO THE CLAIMS:

1. (Currently Amended) An amplifier with a gain proportional to power source voltage comprising:

first and second P-channel MOS field-effect transistors (hereafter abbreviated to MOS-FETs) formed such that respective back gates are electrically isolated from a semiconductor substrate and respective sources are connected in common,

a first voltage source for outputting a voltage obtained by dividing a power source voltage,

a second voltage source for generating a positive voltage having a potential difference almost identical to the threshold voltages of said first and second MOS-FETs with reference to the output voltage of said first voltage source,

a third voltage source for generating a predetermined negative voltage with reference to the output voltage of said first voltage source, and

an operational amplifier, to the positive input terminal of which the output of said second voltage source is applied as a bias voltage, wherein

the sources of said first and second MOS- FETs, connected in common, are connected to the negative input terminal of said operational amplifier,

the respective back gates of said first and second MOS-FETs are connected to either their respective sources or said second voltage source,

the gate of said first MOS-FET is biased at the potential of a circuit ground, and its drain is connected to an input terminal to which a signal with no DC component is input, and

the gate of said second MOS-FET is connected to said third voltage source, and its drain is connected to the output terminal of said operational amplifier coupled to the output terminal [[52]] of said operational amplifier.

2. (Currently Amended) An amplifier with a gain proportional to power source voltage comprising:

first and second N-channel MOS-FETs formed such that respective back gates are electrically isolated from a semiconductor substrate and respective sources are connected in common,

a first voltage source for outputting a voltage obtained by dividing a power source voltage,

a second voltage source for generating a negative voltage having a potential difference almost identical to the threshold voltages of said first and second MOS-FETs with reference to the output voltage of said first voltage source,

a third voltage source for generating a predetermined positive voltage with reference to the output voltage of said first voltage source, and

an operational amplifier, to the positive input terminal of which the output of said second voltage source is applied as a bias voltage, wherein

the sources of said first and second MOS- FETs, connected in common, are connected to the negative input terminal of said operational amplifier,

the respective back gates of said first and second MOS-FETs are connected to either their respective sources or the output terminal of said second voltage source,

the gate of said first MOS-FET is connected to said positive power source voltage, and its drain is connected to an input terminal to which a signal with no DC component is input, and

the gate of said second MOS-FET is connected to said third voltage source, and its drain is connected to the output terminal of said operational amplifier coupled to the output terminal [[52]] of said operational amplifier.

3. (Original) An amplifier with a gain proportional to power source voltage comprising:

first and second P-channel MOS-FETs formed such that respective back gates are electrically isolated from a semiconductor substrate and respective sources are connected in common,

a first voltage source for outputting a voltage obtained by dividing a power source voltage,

a second voltage source for generating, at its output terminal, a positive voltage having a potential difference almost identical to the threshold voltages of said first and second MOS-FETs with reference to the output voltage of said first voltage source,

a third voltage source for generating a predetermined negative voltage with reference to the output voltage of said first voltage source, and

first and second operational amplifiers connected to the output terminal of said second voltage source at respective positive input terminals, wherein

the sources of said first and second MOS- FETs connected in common, are connected to the output terminal of said first operational amplifier,

the respective back gates of said first and second MOS-FETs are connected to either their respective sources or said second voltage source,

the gate of said first MOS-FET is connected to said third voltage source, and its drain is connected to the negative input terminal of said first operational amplifier and to an input terminal to which a signal with no DC component is input,

the gate of said second MOS-FET is connected to a circuit ground, and its drain is connected to the negative input terminal of said second operational amplifier, and

a resistor is connected across the negative input terminal of said second operational amplifier and the output terminal of said second operational amplifier coupled to the output terminal of said operational amplifier.

4. (Currently Amended) An amplifier with a gain proportional to power source voltage comprising:

first and second P-channel MOS-FETs formed such that respective back gates are electrically isolated from a semiconductor substrate and respective sources are connected in common,

third and fourth P-channel MOS-FETs formed so that respective back gates are [[be]] electrically isolated from a semiconductor substrate and respective sources are connected in common,

a first voltage source for outputting a voltage obtained by dividing a power source voltage,

a second voltage source for generating, at its output terminal, a positive voltage having a potential difference almost identical to the threshold voltages of said first, second, third and fourth MOS- FETs with reference to the output voltage of said first voltage source,

a third voltage source for generating a predetermined negative voltage with reference to the output voltage of said first voltage source,

first and second operational amplifiers which are connected in common at respective positive input terminals and biased by said second voltage source,

said first and second P-channel MOS-FETs which are connected in common at respective sources connected to the output terminal of said first operational amplifier, and

said third and fourth P-channel MOS-FETs which are connected in common at respective sources connected to the output terminal of said second operational amplifier, wherein

the respective back gates of said first, second, third and fourth MOS-FETs are connected to either their respective sources or said second voltage source,

the gates of said first and third MOS-FETs are connected to said third voltage source,

the drain of said first MOS-FET is connected to the negative input terminal of said first operational amplifier and to a first input terminal to which a signal with no DC component is input,

the drain of said third MOS-FET is connected to the negative input terminal of said second operational amplifier and to a second input terminal to which a signal with no DC component is input,

the gates of said second and fourth MOS-FETs are connected to a circuit ground,

the drain of said second MOS-FET is connected to the positive input terminal of said third operational amplifier,

the drain of said fourth MOS-FET is connected to the negative input terminal of said third operational amplifier,

said second voltage source is connected to the positive input terminal of said third operational amplifier via a first resistor, and

a second resistor is connected across the negative input terminal of said third operational amplifier and the output terminal of said third operational amplifier coupled to the output terminal of said amplifier.

5. (Original) An angular velocity sensor apparatus comprising:

a drive section for vibrating vibration elements,

a vibration level detection section for detecting the vibration levels of said vibration elements,

Coriolis force detection sections for detecting a Coriolis force generating depending on an angular velocity,

a first amplifier for amplifying the output signal of said vibration level detection section,

a rectifying circuit for rectifying the output signal of said first amplifier to obtain a DC voltage,

a variable gain amplifier, receiving the output signal of said first amplifier, for changing its gain depending on the output value of said rectifying circuit,

a second amplifier for amplifying the output signals of said Coriolis force detection sections,

a phase detector for detecting the phase of the output voltage of said second amplifier on the basis of the vibration frequencies of said vibration elements, and

a DC amplifier for DC amplifying the output of said phase detector, wherein

said second amplifier comprises:

at least two operational amplifiers, and

at least two MOS-FETs in which the drain- source voltage is biased at 0 V, wherein

one of said MOS-FETs is biased so that the gate-source voltage becomes constant, and the other MOS-FET is biased so that the gate-source voltage changes depending on the variation of a power source voltage, and

the gains of said operational amplifiers are determined by the ratio of the channel resistances of said at least two MOS-FETs biased by said voltages different from each other.

6. (Currently Amended) An angular velocity sensor apparatus comprising:

a drive section for vibrating vibration elements,

a vibration level detection section for detecting the vibration levels of said vibration elements,

Coriolis force detection sections for detecting a Coriolis force generating depending on an angular velocity,

a first amplifier for amplifying the output signal of said vibration level detection section,

a rectifying circuit for rectifying the output signal of said first amplifier to obtain a DC voltage,

a variable gain amplifier, receiving the output signal of said first amplifier, for changing its amplification degree depending on the output value of said rectifying circuit,

a second amplifier for amplifying the output signals of said Coriolis force detection sections,

a phase detector for detecting the phase of the output voltage of said second amplifier on the basis of the vibration frequencies of said vibration elements, and

a DC amplifier for DC amplifying the output of said phase detector, wherein

said second amplifier [[42]] comprises:

first [[33]] and second [[34]] P-channel MOS- FETs formed so that respective back gates [[79]] are electrically isolated from a semiconductor substrate [[70]] and respective sources [[76]] are connected in common,

third [[35]] and fourth [[36]] P-channel MOS- FETs so that respective back gates [[79]] are electrically isolated from a semiconductor substrate [[70]] and respective sources are connected in common,

a first voltage source [[11]] for outputting a voltage obtained by dividing a power source voltage [[Vdd]] ,

a second voltage source [[14b]] for generating, at its output terminal [[14h]], a positive voltage having a potential difference almost identical to the threshold voltages of said first, second, third and fourth MOS-FETs with reference to the output voltage [[11a]] of said first voltage source [[11]],

a third voltage source [[12a]] for generating a predetermined negative voltage with reference to the output voltage [[11a]] of said first voltage source [[11]],

first [[66]] and second [[67]] operational amplifiers which are connected in common at respective positive input terminals [[(+]] and biased by said second voltage source [[14b]],

said first [[33]] and second [[34]] P-channel MOS-FETs which are connected in common at respective sources connected to the output terminal of said first operational amplifier [[66]],

said third [[35]] and fourth [[36]] P-channel MOS-FETs which are connected in common at respective sources connected to the output terminal of said second operational amplifier [[67]],

the respective back gates of said first, second, third and fourth MOS-FETs are connected to either their respective sources or said second voltage source [[14b]],

the gates of said first [[33]] and third [[35]] MOS-FETs are connected to said third voltage source [[12a]] ,

the drain of said first MOS-FET [[33]] is connected to the negative input terminal [[(-)]] of said first operational amplifier [[66]] and to a first input terminal [[53]] to which a signal with no DC component is input,

the drain of said third MOS-FET [[35]] is connected to the negative input terminal [[(-)]] of said second operational amplifier [[67]] and to a second input terminal [[54]] to which a signal with no DC component is input,

the gates of said second [[34]] and fourth [[36]] MOS-FETs are connected to a circuit ground,

the drain of said second MOS-FET [[34]] is connected to the positive input terminal [[(+)]] of said third operational amplifier [[68]],

the drain of said fourth MOS-FET [[36]] is connected to the negative input terminal [[(-)]] of said third operational amplifier [[68]],

said second voltage source [[14b]] is connected to the positive input terminal [[(+)]] of said third operational amplifier [[68]] via a first resistor [[49]], and

a second resistor [[50]] is connected across the negative input terminal [[(-)]] of said third operational amplifier [[68]] and the output terminal of said third operational amplifier [[68]], which leads to the output terminal [[55]] of said amplifier. ~~(FIG. 8, FIG. 9)~~